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EXAMINER	
VOCKRODT, JEFF B	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,127	ASSADERAGHI ET AL.	
	Examiner	Art Unit	
	Jeff Vockrodt	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18* is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to the amendment filed on June 19, 2003. Claims 1-18 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,266,821 ("Chern '821") in view of U.S. Pat. No. 4,929,989 ("Hayano").

Chern '821 teaches a depletion type MOS capacitor that is used as a decoupling capacitor. Reference is made to Figs. 8-9, claim 1 of Chern '821, and col. 3, ll. 44-48.

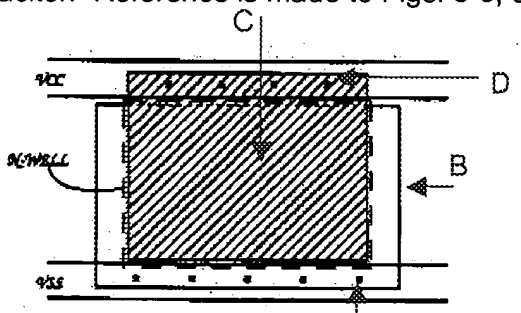

Fig. 8

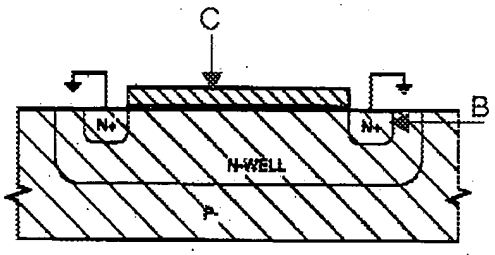

Fig. 9

Findings Re: Chern '821

1. Figs. 8-9 describe depletion mode transistors (col. 3, ll. 44-46) (*Figs. 8-9 above have been modified by adding labels to clarify discussion of the figures*).

2. Fig. 8 is a plan view, while Fig. 9 is a cross-sectional view at a location between the VCC and VSS lines. The examiner has added labels to help explain the understanding of the reference.

A: points to the solid squares at the lower portion of the device body, which the examiner understands to be contact vias extending between the Vss wire and the N+ region in the substrate.

B: points to the solid-rectangular line that overlaps the Vss line and surrounds the solid square contact vias that are labeled A.

C: points to the polysilicon upper capacitor electrode.

D: points to the solid squares at the upper portion of the device body, which the examiner understands to be contact vias extending between the Vcc wire and the polysilicon upper capacitor electrode (labeled C).

3. The N-well is labeled inconsistently between Fig. 8 and Fig. 9. The line connecting the "N-WELL" label of Fig. 8 to a dash region that is nearly co-extensive with the polysilicon gate is clearly a drafting error since the Vss region would contact neither the N-well nor the N+ regions and would not be in contact with the lower capacitor electrode. It appears that this line was simply added in error because the location of the N-well label (without line) in Fig. 8 is consistent with the location of the N-well in Fig. 9. That is, the N-well is outside of the N+ region and surrounds the N+ region. The boundary between the p- region and the n-well region is outside of the region depicted by Fig. 8 or is simply not shown. With this understanding, the dashed line connected to the n-well label likely corresponds to the capacitor dielectric which is co-extensive with the upper capacitor electrode in both Figs. 8-9.

4. Fig. 9 shows the lower capacitor plate (N-well and N+ region) connected to the ground ("one node is tied directly to the substrate"; claim 1, clause (d)). Vss denotes a ground terminal. Fig. 9 shows contacts (herein labeled A) that extend between Vss and a region of the substrate (herein labeled B). Fig. 9 shows diagrammatically that the N+ regions are connected to the ground terminal. Fig. 8 shows that Vss (ground terminal) is connected to region (B), but does

not state what region (B) is. Region (B) in Fig. 8 corresponds to the N+ region in Fig. 9 since (1) both are connected to the ground terminal (Vss), (2) both appear to be aligned to the polysilicon layer in a manner that is commonly known for doping source/drain regions in the MOSFET context, and (3) the labeling of the N-well in Fig. 8 is clearly a drawing error and is properly given little weight in understanding Figs. 8 and 9. The capacitor plate (herein labeled C) is tied ("tied . . . directly to Vcc power bus") to the power bus by way of contacts (herein labeled D) of Fig. 8.

5. Summarizing, Chern '821 teaches:

> electrically connecting the first and second lateral regions (N+ regions) to a first supply voltage potential (Vss) at a first longitudinal end of the device body (solid square N+ contacts at the lower side of the device body in Fig. 8); and electrically connecting the electrode layer (polysilicon electrode) to a second supply voltage potential (Vcc) at a second longitudinal end of the device body opposite to the first longitudinal end of the device body (solid square contacts at the upper side of the device body, Fig. 8).

Claim 1 corresponds to Chern '821 as follows (differences underlined): A method of forming a capacitor (Figs. 8-9) on a semiconductor substrate, the method including the steps of: (a) forming a device body (N-WELL; Figs. 8-9) in the semiconductor substrate using a first type (N-type) of dopant material; (b) forming a dielectric layer ("oxide" or capacitor insulator; col. 3, ll. 10-11) over the device body; (c) forming an electrode layer (poly 25; compare Figs. 4 and 9) over the dielectric layer in an area defined by an upper surface of the device body (Fig. 9); (d) forming a first lateral region (leftmost N+ diffusion; Fig. 9)in the semiconductor substrate along a first lateral side of the device body (N-WELL), the first lateral region being in electrical contact with the device body along the first lateral side of the device body and containing the first type of dopant material at a level relatively higher than is characteristic of the device body (Fig. 9); (e) forming a second lateral region (rightmost N+ diffusion; Fig. 9) in the semiconductor substrate along a second lateral side of the device body opposite the first lateral side, the second lateral

region being in electrical contact with the device body along the second lateral side of the device body and containing the first type of dopant material at a level relatively higher than is characteristic of the device body (N+ versus N); (f) forming an insulating layer over the electrode layer, first lateral region, and second lateral region; (g) electrically connecting the first and second lateral regions (15; Fig. 4) to a first supply voltage potential at a first longitudinal end of the device body (connection to Vss; Figs. 4 and 8); and (h) electrically connecting the electrode layer (25; Fig. 4) to a second supply voltage potential at a second longitudinal end of the device body opposite to the first longitudinal end of the device body (connection to Vcc; Figs. 4 and 8).

Chern '821 discloses that the busses to which the first and second lateral regions and the electrode are connected, "are typically metallization layers," col. 3, ll. 15, but does not state the claim requirement of "(f) forming an insulating layer over the electrode layer, first lateral region, and second lateral region." It is noted, however, that the black squares in Fig. 4 suggests connecting the metallization to the device at those locations. The claim limitations would be fully met by depositing an insulating material over the entire substrate surface prior to forming the metallization layers for the busses in the process of Chern '821.

Hayano teaches MOS type decoupling capacitors connected between Vcc and ground and interconnected using a metallization structure (Figs. 1A-1B). Hayano teaches interposing an insulating layer (5) between the metallization (37, 39) and upper (34) and lower (3) electrodes. One of ordinary skill in the art would recognize from Hayano that using an insulating layer allows for more sophisticated interconnect layout and enables contacting the device through contact holes at predetermined locations.

Chern '821 and Hayano are analogous art and in applicant's field of endeavor -- MOS type decoupling capacitors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to deposit an insulating layer over the entire decoupling capacitor before forming the metallization layer in the process of Chern '821. One of ordinary skill in the art would have been motivated to interpose an insulating layer between the metallization and the MOS capacitor to provide for more sophisticated interconnect layout and enable contacting the device through contact holes at predetermined locations as taught by Hayano.

Claim 4. The method of claim 1 further including the step of forming a first end region (region where contacts to Vss are made; Fig. 8) in the semiconductor substrate abutting the first longitudinal end of the device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the device body, the first end region being formed using the first type of dopant material.

Claim 5. The method of claim 4 wherein the step of electrically connecting the first lateral region and the second lateral region to the first supply voltage potential comprises forming ground potential contacts to the first end region (This is shown by symbols on Fig. 9 and the actual contact region in Fig. 8).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 6,018,175 ("Kao") (cited in IDS filed March 6, 2002).

Claim 2. The method of claim 1 wherein the first type of dopant material comprises N-type material and the step of forming the device body includes implanting the N-type material in a bulk P-type semiconductor substrate. (Chern '821; Fig. 9).

The only difference between Chern '821 and Hayano as applied to claims 1, 4, and 5 above and the subject matter of claim 2 is that Chern '821 does not teach whether the dopant regions, specifically the N-WELL region, is formed using ion implantation.

Kao teaches a well-implant step after forming the oxide and before forming the first mask (col. 5, ll. 18-28) in forming a depletion mode capacitor.

It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out the formation of the N-WELL region using ion implantation in the process of Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to use ion implantation by Kao's teaching that well-implantation was well known and desirable for forming n-well regions in MOS decoupling capacitors.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 5,965,928 ("Nagura").

Chern '821 differs from claim 3 by not teaching "(b) wherein the step of forming the device body includes performing an additional N-type material implantation in a selected area of the well." Instead, Chern '821 teaches only one doping step for forming the body of the capacitor.

Nagura teaches an improvement on MOS capacitors (Fig. 1E) that includes forming n-type diffusion regions (17; Fig. 1F) in n-type well regions (4) between lateral doping regions (20). Nagura teaches that this suppresses the voltage dependence of the capacitance (e.g., col. 3, ll. 59-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a step for forming diffusion region in the device by implanting an additional n-type material into the well in the process taught by Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to include this step because such structure was known to reduce the voltage dependence of the capacitance as taught by Nagura.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 6,034,388 ("Brown").

Claim 6. The method of claim 1 further including the steps of forming a buried oxide layer in the semiconductor substrate and forming side oxide regions in the semiconductor substrate in areas bounding an area for the capacitor, the steps of forming the buried oxide layer and side oxide regions being performed prior to forming the device body. Claim 6 differs from Chern '821 and Hayano as applied above by requiring a buried oxide layer and side oxide regions.

Brown teaches forming a depletion mode capacitor in a SOI substrate that includes buried oxide regions (522; Fig. 13) and side oxide regions (shallow trench isolation 170; Fig. 13) which are formed prior to forming the device body (520). Brown teaches that using SOI increases the resistance (col. 14, ll. 38-39).

Chern '821, Hayano, and Brown are within the same field of endeavor as applicant -- MOS type decoupling capacitors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the decoupling capacitor of Chern '821 and Hayano on a SOI substrate having side oxide regions formed prior to the body formation. One of ordinary skill in the art would have been motivated to use SOI by the expectation of increased resistance as taught by Brown.

Claims 7-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821, Hayano, and Brown as applied to claim 6 above, and further in view of Kao.

Chern '821, Hayano, and Brown differ from claims 7-8 and 10-11 in that Chern '821 does not teach ion implantation and is silent as to the doping method. Kao as applied to claim 2

above teaches how to use ion implantation to form the device of Chern '821. The findings with respect to claim 2 above are incorporated in this section. It would have been obvious to one of ordinary skill in the art at the time of the invention to carry out the formation of the N-WELL region using ion implantation in the process of Chern '821, Hayano, and Brown. One of ordinary skill in the art would have been motivated to use ion implantation by Kao's teaching that well-implantation was well known and desirable for forming n-well regions in MOS decoupling capacitors.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821, Hayano, Brown, and Kao as applied to claims 7-8 and 10-11 above, and further in view of U.S. Pat. No. 5,965,928 ("Nagura").

Chern '821 differs from claim 9 by not teaching "(b) wherein the step of forming the device body includes performing an additional N-type material implantation in a selected area of the well." Instead, Chern '821 teaches only one doping step for forming the body of the capacitor.

Nagura teaches an improvement on MOS capacitors (Fig. 1E) that includes forming n-type diffusion regions (17; Fig. 1F) in n-type well regions (4) between lateral doping regions (20). Nagura teaches that this suppresses the voltage dependence of the capacitance (e.g., col. 3, ll. 59-61).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide a step for forming diffusion region in the device by implanting an additional n-type material into the well in the process taught by Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to include this step because such structure was known to reduce the voltage dependence of the capacitance as taught by Nagura.

Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821 and Hayano as applied to claims 1, 4, and 5 above, and further in view of U.S. Pat. No. 5,032,892 ("Chern '892).

Claim 12 differs from Chern '821 since Chern '821 does not teach concurrently forming a capacitor device body and a plurality of additional device bodies and does not teach step (d) of claim 12.

Chern '892 teaches forming a PMOS transistor (121, 131, 132) while forming a n-doped depletion mode capacitor (139). Chern '892 corresponds to step (d) of claim 12 as follows: (d) forming a first lateral region (134) and a second lateral region (135) in the semiconductor substrate along opposite lateral sides of the capacitor device body (113) and concurrently forming a respective drain region (131) and a respective source region (132) in the semiconductor substrate for a number of the second type circuit devices, the first lateral region (134) and second lateral region (135) being formed using the first type of dopant material a level relatively higher (indicated by "+" signs, e.g. n+) than is characteristic of the capacitor device body (113). Chern '892 teaches that "a separate depletion mask is not needed in a CMOS process because one can introduce n-type doping to form the n doped barrier during the n well implant step" (¶ bridging cols. 4-5).

It would have been obvious to one of ordinary skill in the art at the time of the invention to concurrently form a capacitor device body (n doped barrier) and a plurality of additional device bodies (n wells) in the process of Chern '821 and Hayano. One of ordinary skill in the art would have been motivated to make this modification to eliminate the separate depletion masking step as taught by Chern '892.

Claim 14. The method of claim 12 wherein the step of forming the first lateral region, second lateral region, each drain region, and each source region also includes concurrently

forming a first end region (region where contacts to Vss are made; Chern '821, Fig. 8) in the semiconductor substrate abutting the first longitudinal end of the capacitor device body and contacting the first and second lateral regions adjacent to the first longitudinal end of the capacitor device body.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chern '821, Hayano, and Chern '892 as applied to claims 12 and 14 above, and further in view of Kao.

Claim 13 requires implanting the dopants. See treatment of claim 2 in view of Kao above for reasons underlying this ground of rejection.

Allowable Subject Matter

Claim 18 is allowed.

Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments directed to claims 1-14, which were filed June 19, 2003, have been fully considered but they are not persuasive.

Claims 1-14 have been rejected under 35 U.S.C. § 103(a) in view of U.S. Pat. No. 5,266,821 ("Chern '821) in view of other references. Applicant concludes that Chern '821 does not teach steps (g) and (h) of independent claim 1 and similar limitations of claim 12. The examiner has reviewed Chern '821 in light of applicant's arguments, but is unable to reach the same conclusion as applicant with respect to the Chern '821 reference.

Applicant states: "Figure 8 of the 821 patent appears to show Vss connections at outside the N-well of the device structure." If it is true that Vss connections are outside of the N-well structure, then the lower capacitor electrode (diffused regions) would not be connected to Vss

(ground terminal). However, it is abundantly clear from Chern '821 that the lower capacitor electrode must be connected to Vss (ground terminal) to result in an operative depletion mode capacitor. (see claims 1 and 3 of Chern '821, Vcc (power bus), Vss (ground potential)). Accordingly, this ambiguity in the drawings does not render the above findings incorrect.

Applicant states: "The Examiner also suggested that Figure 8 of the 821 patent is mislabeled and that the N-well in the structure in fact comprises the solid rectangle rather than the dashed rectangle shown in the drawing." This is incorrect since the solid rectangle in Fig. 8 corresponds to the N+ regions in Fig. 9. The border between the N-well and the p-substrate is not shown in Fig. 8 or it is outside of the area depicted in the figure.

It is acknowledged that Chern '821 is objectionable in that the figures are poorly labeled. However, Chern '821 is not ambiguous. See In re Hughes, 345 F.2d 184, 145 USPQ 467 (CCPA 1965) (anticipation rejection improper where reference discloses two possibilities only one of which meets the claim language). The only reasonable interpretation of Chern '821 leads to a device (and process of forming) that fully meets the disputed claim limitations at the level of specificity required by the claims. The examiner has provided findings of fact in connection with the statement of rejection that interpret Chern '821 as it would have been understood by a person of ordinary skill in the art at the time of the invention (i.e., applicant's effective filing date). The examiner believes that those findings are supported on this record by substantial evidence. Accordingly, the rejection of claims 1-14 as set forth above is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning communications from the examiner should be directed to Jeff Vockrodt at (703) 306-9144 who can be reached on weekdays from 9:30 am to 5:00 pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian, can be reached at (703) 308-4905.

The fax numbers for this Group are (703) 305-3432, (703) 308-7722, (703) 305-3431, and (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist at (703) 308-0956.

August 27, 2003
J. Vockrodt

AMIR ZARABIAN
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